Ageing Simulation of Analogue Circuits and Systems using Adaptive Transient Evaluation

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***Abstract*—Simulating ageing effects in analogue circuits requires both ageing models and a circuit simulator which is capable of a stress dependent, ageing and recovery aware model evaluation during long term transient simulation. Common approaches on reliability simulation often involve aged models, age precomputation, or lookup tables instead of integrated ageing simulation using memory aware ageing models. Long term transient ageing simulation enhances reliability simulation. This paper presents a framework to model and simulate ageing effects using an adaptive two-times evaluation scheme. This integrates full ageing effect models into behavioural device models. In addition, we introduce semantics for modelling stress levels and ageing parameters in hardware description languages. Our approach is a fully integrated simulation solution, enabling correct and efficient simulation of ageing systems over their lifetimes. We demonstrate how transistor level ageing effects critically affect the operation of a circuit. Our examples incorporate ageing monitors, redundant parts, and self-repair functionality into analogue systems.**

I. Introduction

With increasing integration, ageing effects in electronics introduce lifetime issues. Ageing causes a continuous change of behavioural properties [1]. Often, exposure to stress is responsible and a different stress impact causes differently altered components. Hot carrier injection (HCI) [2] and (negative) bias temperature instability (N)BTI [3] are MOSFET ageing mechanisms. These are subject to the voltages applied to the transistors, and hence depend on the transient operation the whole circuit performs. This is most relevant in analogue circuits, where voltage levels may vary widely due to ageing, and performances are sensitive to parameters.

Current research on reliability evaluation imposes the concept of 'mission profiling' [4] to systems. A mission profile specifies the (expected) influences on a system in terms of input signals or levels and environmental conditions on a lifetime scale. Evaluating a system during such a mission involves modelling and simulation challenges. Parameter optimization strategies targeting performances or yield depend on numerical nominal simulation results. Accuracy and speed are critical for the search algorithms.

Physics based simulations reveal the impact on transistor circuits [5], [6]. Recent results [7] show how precomputed fast components of NBTI affect analogue SPICE simulations. For long term considerations, such as implied by mission profiles, neither precomputation nor curve fitting techniques are valid, hence ageing models and circuit simulation need to be reasonably coupled. Nominal ageing simulation can be done by simulating short transients at different times T_i, evaluating the ageing models and tracking the impact on the circuits behaviour. Seperate ageing model evaluation and ad-hoc simulation loops involving SPICE are common practice e .g. in [8]. Embedded stress level and event-aware step control or efficiency has not been considered yet. Circuit level and system simulation requires faster and higher level ageing models. Available hardware description languages do not provide semantics for ageing effects. Existing workarounds include extra voltage sources [9], or time scaling [10]. Available low level model interfaces in commercial reliability simulators lack expressiveness. Basically, existing approaches do not allow for either accurate modelling or lack efficient long term simulation.

Our contribution is an ageing simulation technique that

- provides nominal analogue circuit and analogue ageing effect evaluation,
- computes long term transients efficiently,
- incorporates an ageing state and stress level and event aware step control,
- enables ageing effects in behavioural models and
- has been implemented as proof of concept based on free software.

II. Ageing Effects

An *ageing parameter* p describes a property of a circuit subject to change depending on how the circuit is exposed to stress during its lifetime. We define an *ageing state* as a variable value which is subject to change according to a stress *level*. Without loss of generality, we let a lower state correspond to a fresher condition. Similarly, a stress level is a variable which depends on the current transient state. A negative rate corresponds to recovery.

The ageing parameter, such as an interface trap state or a behavioural parameter (e. g. an offset shift), is associated to a state vector $\mathbf{z} = [z_1, \dots z_n]^t$. Each state is controlled by a stress level, a time dependent function $L\colon [0,t] \to \mathbb{R}$. We write L_T for the stress level profile restricted to the time interval $[0,T]$ and $z(T) = z(L_T)$ for the value of the state z after the influence of L_T. Finally, an ageing parameter is a function $p(\mathbf{z})$ of the state vector.

A. Controlling Decay Processes

Two rate controlled decay processes acting on a set of states in opposed directions form a stochastic process (Fig. 1). This **R**eversely **C**oupled **D**ecay (RCD) process is suited to model

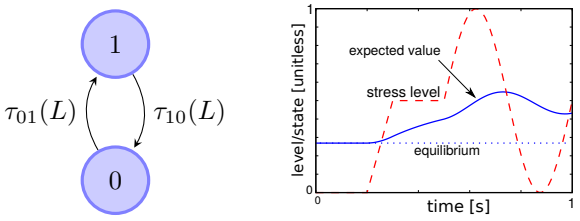

Fig. 1. Example RCD. A stress signal (dotted) and its effect on the expected value of the process. Here, $\tau_{01} = \exp(1 - L)\,\mathrm{s}$ and $\tau_{10} = \exp(L)\,\mathrm{s}$.

time continuous, analogue stress level controlled and recovery aware ageing parameters such as BTI [11]. Its expected value is the defect state z. The equilibrium at stress level 0 is the initial (fresh) value. Exponential functions work well to express the dependency between stress level and transition rate, as they are smooth, always positive and strictly monotonic. If L is a stress level, the half live times τ_{01} and τ_{10} in seconds may be chosen as $\exp(a \cdot L + b)$ with positive (resp. negative) a for the transition $0 \to 1$ (and $1 \to 0$ respectively) and suitable b.

III. Simulating Ageing Effects

Roughly, an FET is a controlled current source with value $I_{\mathrm{DS}} = K \cdot (V_{\mathrm{GS}} - V_{\mathrm{th}})^2$, where K is a constant. Some ageing effects cause a gradual shift in threshold voltage V_{th}. With the notions from Section II, the threshold voltage is a function p of the state $\mathbf{z}(t)$ which is to be determined by the level of stress until t. For simplicity, let $\mathbf{z}$ be just $[z] \in \mathbb{R}^1$ and only depend on $\mathbf{L} = [L] = V_{\mathrm{GS}}/\mathrm{V}$, then $V_{\mathrm{th}}(t) = V_{\mathrm{th},0} + \Delta V_{\mathrm{th}} = p(z(L_t))$ For multiple components, we get equations $\mathbf{f}_{\mathrm{m}}$ describing the circuit with the state $\mathbf{x}$ for the node voltages with a dependency on the ageing states $\mathbf{z}$. Ageing states move slower than node voltages, hence the differential equation may be written as

$$\begin{aligned} \mathbf{x}(0) &= \mathbf{x}_0 \\ \mathbf{f}_{\mathrm{m}}\left(\mathbf{x}(t), \partial\mathbf{x}(t)/\partial t, \ldots, t, \mathbf{z}(t)\right) &= 0 \\ \mathbf{z}(0) &= 0 \\ \mathbf{f}_{\mathrm{a}}\left(\mathbf{L}(\mathbf{x}(t)), \mathbf{z}(t), \partial\mathbf{z}(t)/\partial t\right) &= 0. \end{aligned} \tag{1}$$

The function $\mathbf{f}_{\mathrm{a}}$ holds the equations for the ageing states.

In the above example, V_{th} is shifted by an RCD controlled by $L = V_{\mathrm{GS}}/\mathrm{V}$, the differential equation for z turns out to be $\mathbf{f}_{\mathrm{a}} = \partial z/\partial t + c_1(V_{\mathrm{GS}}/\mathrm{V}) \cdot z + c_0(V_{\mathrm{GS}}/\mathrm{V})$ [11]. In Fig. 1 we have $c_1 = \tau_{01}^{-1} + \tau_{10}^{-1}$ and $c_0 = \tau_{10}^{-1}$.

We require that for an aging effect model, a notion of average stress $\overline{L}$ exists. Average stress describes the stress impact during short intervals and is locally stable. This exists for integrating models such as $p(\mathbf{x}_T) = p\left(\int_0^T L(\mathbf{x}(t))\mathrm{d}t\right)$. RCD processes support an average with similar properties, the *equivalent constant stress* [12]. The interrelation between $\overline{\mathbf{L}}$ and $\mathbf{z}$ permits the application of predictor-corrector methods and provides step control measures.

A. A Two-Times Simulator

We compute transients of systems of type of Eq. 1. We factor absolute time into $t + T$, where t represents the transient, *first-time* and T is the age or *second-time*. Transient simulations, *frames*, are executed at increasing second-times T_i, these may vary in length.

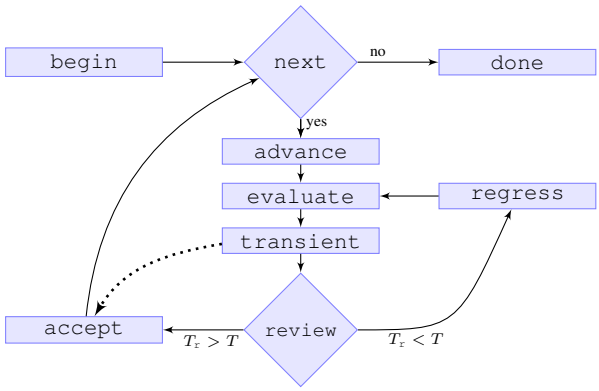

Fig. 2. Adaptive ageing simulation algorithm, naming adopted from Gnucap transient simulation. Dotted bypass: conventional simulation, effectively.

```
model ageing_mosfet(d, g, s, b);
  electrical d, g, s, b;
  degradational hci, bti0, .. btik;
  [ parameters, variables, functions .. ]
  tt_int hci_integrator(hci);
  rcd_exp #(..) rcd0(bti0), .., #(..) rcdk(btik);
  analog begin
    vth = ..;
    vth *= ( 1 + State(hci)**hci_n
             + State(bti0) + .. + State(btik));
    I(d,s) <+ K * (V(g,s) - vth)**2;
    Level(hci) <+ hci_fct(V(d),V(g),V(s),V(b));
    Level(bti0) <+ V(g,s);
    ..
    Level(btik) <+ V(g,s);
  end
endmodel
```

Fig. 3. Verilog-A implementation of an FET affected by BTI and HCI, simplified for readability. The subdevices used for integration (`tt_int`) and decay process evaluation (`rcd_exp`) are not specific to defect mechanisms.

The times are controlled by the respective `next` routines. The second-time T is fixed to the begin of the frame that is currently simulated. The ageing components collect stress levels at each transient step the simulator accepts. The last accept within a frame computes $\overline{L}$. The algorithm that controls the second-time is close to a transient simulation loop (Fig. 2). This involves a `review` procedure, where the components determine their individual maximum tolerable second-time step or schedule events. The discrepancy between the extrapolated average $\overline{\mathbf{L}}_{\mathrm{e}}$ to $\overline{\mathbf{L}}_{\mathbf{z}}$, the average computed from the extrapolated ageing state, is relevant. In the second order case, $\overline{L}_{\mathrm{e}}$ is obtained using quadratic extrapolation, the `review` demands $T_{\mathrm{r}} \leq \mathrm{tol}/\left(\overline{L}_{\mathrm{e}}(T) - \overline{L}_{\mathbf{z}}(T)\right)^{1/2}$ for the entries L of $\mathbf{L}$.

B. Behavioural Modelling

The inner workings of an ageing parameter model is beyond the expressive power of widespread hardware description languages. We add the semantics of ageing effects into behavioural modelling languages by means of subdevices and a specially crafted node type (see Fig. 3). Then, using a stress integrator (`tt_int`), we model ageing effects such as HCI. Other effects, particularly those involving recovery, can be expressed with decay process subdevices. The computation of stress levels from transient states or parameter shifts from states $\mathbf{z}$ does not require language extensions. To represent

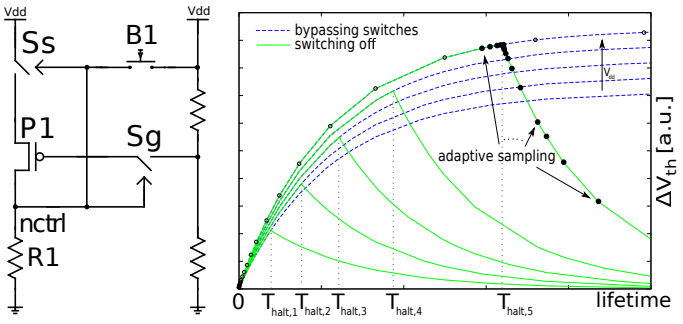

Fig. 4. The Halting Problem. The voltage at nctrl controls the switches Sg and Ss. $|\Delta V_{th}|$ in P1 varies over time, and causes a shutdown. Circles mark the computed second-time steps, those at filled circles are introduced by the shutdown.

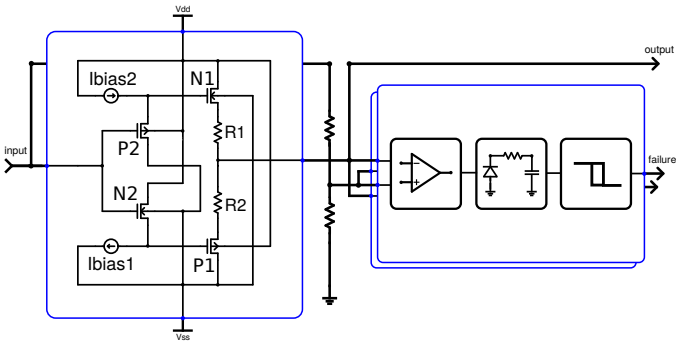

Fig. 5. A power stage with a peak-error window detector.

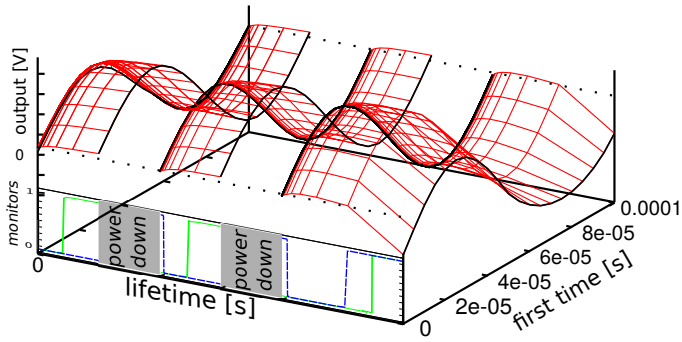

Fig. 6. Monitoring the power stage: The failure signals (front) indicate too high (green) and too low (blue, dashed) offset peaks.

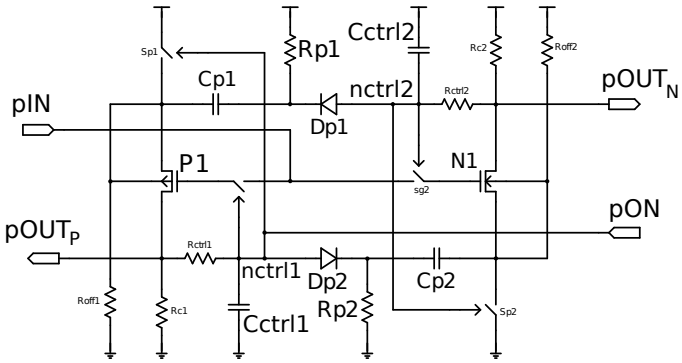

Fig. 7. A simplistic embedded redundancy circuit. This circuit is symmetric except for the different ageing effects in N1 and P1.

stress `Level` and ageing `State`, we stretch the notion of conservative signal flow, defining natures with the corresponding accesses. Model compiler and simulator are aware of the so defined discipline.

IV. Applications

We use BSIM 3.3 transistors augmented with HCI and BTI effect models as shown in Fig. 3. The BTI model consists of eight RCD processes spanning eleven decades of effective half live time. For efficiency, we have also incorporated functionally equivalent ageing parameters and subdevices into the C++ code of an existing BSIM 3.3 implementation. Our implementation is based on AdmsXML [13] and Gnucap [14].

A. Circuit Examples

Consider the **Halting Problem** circuit (Fig. 4, left). The switches Sg and Ss are voltage controlled, are on at high voltage and have the same threshold. Pushing button B1 enables P1. P1 and R1 are chosen, such that ageing causes the voltage at nctrl drift below the switching threshold, shutting down the circuit. The time of shutdown depends on the degradation state of P1. Its ageing state depends on the stress history. We activate B1 once, at time 0 and simulate until P1 switches itself off. The halting time still depends on the supply voltage. A higher supply voltage causes the transistor to age faster, but then also more damage is required to reach the threshold of Sl and Sg.

Monitor circuits can be used to detect circuit failures [15]. Long-term ageing simulation enables the development of analogue on-line monitors. The circuit in Fig. 5 implements an offset monitor connected to a power stage built from source followers. The power stage is symmetric, except for the p- and n-FETs interchanged. These are subject to HCI and NBTI stress. As the nFETs age, the offset voltage lowers, and higher damage on the p-FET side causes a higher offset. A lower levelled signal has more effect on the nFETs, especially on N2. At the beginning, the output offset is rising due to NBTI in P1 and P2. later, HCI catches up. Two monitors track the offset deviation comparing output with the input voltage. Inside the monitor, a trigger is connected to a control node that holds a low-passed peak-difference. Two monitors with interchanged input polarity report too high and too low peak-level offset. In Fig. 6 the circuit is simulated with a sine input signal to the power stage. Power down phases, such as prescribed by a mission profile, interrupt the operation.

Cross coupling two instances of the Halting Circuit we build a **redundant circuit** (Fig. 7). The instance on the right side uses an nFET. Pulling up the control node (via pON), turns on the unit on the left. The input applied to pIN is an analog signal chosen such that the fresh FET P1 keeps the voltage at nctrl1 above the power-off threshold. This voltage, the low-passed output voltage, will drift down as P1 ages. Consequently, the power supply for the left unit will switch off at some time, pulling down Dp1 through a high pass (Cp1, Rp1), activating the complementary unit on the right. During the operation on the right side, P1 is off and recovering from

TABLE I. RUN TIMES AND DIRECTED HAUSDORFF DISTANCES TO FINE SAMPLING OF THE EXAMPLE CIRCUITS.

Sampling	Common Source nFET			Halting Circuit			Monitored Amp			Redundancy		
Reference	4.3 h	ΔV_{th}	V_{gs}	16 h	ΔV_{th}	V(nctrl)	23 h	ΔV_{th}(N2)	V(nctrl)	14h	V(nctrl1)	V(nctrl2)
Adaptive	5 ms	0.42 %	0.18 %	1.7 s	0.01 %	0.1 %	44.3 s	0.41 %	1.2 %	7.5 min	0.24 %	0.18 %
Equidistant	7 ms	2.95 %	1.70 %	1.5 s	1.3 %	4.5 %	16.8 min	0.23 %	3.3 %	3.2 h	4.9 %	8.3 %
Exponential	11 ms	13.96 %	7.99 %	1.6 s	4.9 %	6.3 %	50.4 s	4.85 %	10.2 %	N/A	N/A	N/A

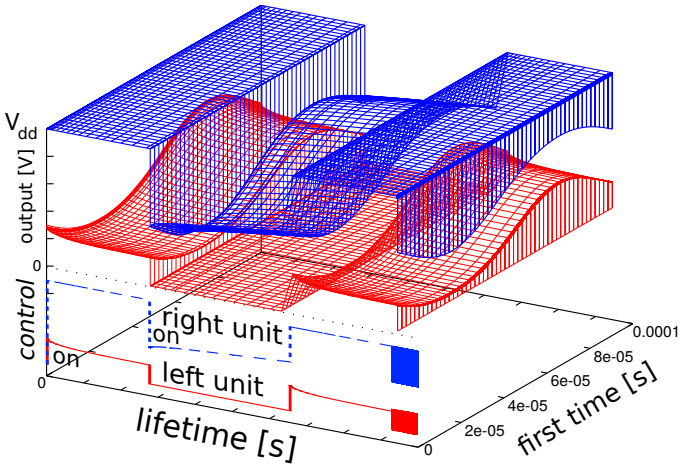

Fig. 8. Output and control voltages during simulation. The circuit is processing a sine-waved signal at pIN.

NBTI. Thus, at the time the right unit breaks down, the left unit will take over. The takeover works similar, with directions interchanged. As N1 does not recover from HCI, the third breakdown will be definite. Here, the voltages controlling the switches do not solely depend on the ageing state. Due to the alternating voltages, the charges on the capacitors Cctrl1 and Cctrl2 are volatile. Over- and underestimating these charges during second-time extrapolation will distort the simulation results. The trend of a capacitors charge becomes a component of the state vector $\mathbf{z}$. We extrapolate the charges on capacitors from the data collected by transient simulations (Fig. 8).

B. Results

Let f be a sampled real valued function on a bounded subset of the real numbers. The sampling of f gives rise to the set of sample points $S_f = \{(x, f(x)) \mid f \text{ sampled at } x\} \subset \mathbb{R}^2$. Assume S_f has nonzero height and width. A transformation A_f scales and translates S_f into the unit square such that all edges are hit. Let g be another function. We define the *normalized directed discrete Hausdorff-distance* $\mathrm{dhdd}(f, g)$ to be the directed Hausdorff distance $\mathrm{dhd}(A_f(S_f), A_g(S_g))$ from [16]. We compare results obtained using different sampling strategies with an excessively finely sampled reference. Adaptive sampling is the proposed strategy. Equidistant and exponentially growing time steps are chosen to produce comparable results. Table I lists run times (on a 2.2 Ghz CPU) and $\mathrm{dhdd}(p_s, p_{\text{fine}})$ for probes p and strategies s. We include the single nFET common source circuit taken from [9]. The others are from Section IV. Here, the monitored power stage has been simulated without the power-down phases. The embedded redundancy circuit does not simulate with huge time steps, hence the exponential sampling is not applicable. Summarizing, adaptive sampling greatly improves accuracy and run times.

V. CONCLUSION

As the influence of ageing effects is growing with decreasing structure size, accurate nominal simulation and modelling techniques are inevitable. This involves proper algorithms such as two-times simulation of arbitrary ageing effects as well as integration of suitable effect models into hardware description languages. In this paper, we point to a common denominator of ageing effects, behavioural modelling and circuit simulation. On top of this, we have developed a stress level aware adaptive step control scheme to simulate circuits involving aging effects. This demonstrates feasibility and opens up new possibilities for future reliability studies.

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